REMARKS

Claims 1-6, 25 and 26 are pending in the application, with claims 1 and 2 being independent. Claim 2 has been amended to correct minor errors. No new matter has been introduced.

Claims 1, 3, 5 and 6 have been rejected as being unpatentable over Suzawa, JP 2001-035808 in view of Hibino, JP 2001-010685. Applicant requests reconsideration and withdrawal of this rejection because neither Suzawa nor Hibino would have provided any motivation for one of ordinary skill in the art to combine Suzawa and Hibino in the manner suggested by the Examiner. In particular, in contrast to the subject matter of claim 1 and Suzawa, both of which are directed to a structure in which a gate electrode is formed over a semiconductor layer that includes, for example, a channel formation region, Hibino is directed to a stagger-type TFT having a gate electrode formed below the semiconductor layer. As such, since Hibino is directed to an entirely different arrangement of the gate electrode relative to the semiconductor layer, nothing in Hibino would have motivated one of ordinary skill in the art to employ Hibino's gate electrode in Suzawa's device.

Moreover, while the Examiner argues that the motivation would have come from Hibino's teaching that the use of three layers helps to prevent erosion of the gate electrode, applicant respectfully disagrees. Suzawa describes a gate electrode that includes a tungsten nitride film 603b as a lower layer and a tungsten film 603a as an upper layer. By contrast, Hibino employs a structure that includes an Al film 14 sandwiched between a Ti film 13 and a TiN film 15. While Hibino states that this structure helps prevent erosion of an Al film during etching, prevention of such erosion would not have provided the necessary motivation since Suzawa does not use an Al film as the gate electrode and, accordingly, does not face the erosion problem described by Hibino. Indeed, given Suzawa's criticism of the use of Al films, Suzawa would have motivated one of skill in the art away from using the electrode structure described by Hibino in Suzawa's system.

For at least these reasons, the rejection should be withdrawn.

Claims 2, 4, 6 and 26 have been rejected as being unpatentable over Suzawa in view of Yudasaka, U.S. Patent No. 5,953,582, and further in view of Hibino. Like claim 1, independent claim 2 recites a gate electrode formed from three layers. Accordingly, applicant requests reconsideration and withdrawal of this rejection because Yudasaka '582 does not remedy the failure of Suzawa and Hibino to provide motivation for using Hibino's electrode in Suzawa's system.

The claims have been rejected for obviousness-type double patenting over claims 1, 3 and 7 of Yudasaka, U.S. Patent No. 6,657,260. Applicant requests reconsideration and withdrawal of this rejection because, as noted by the Examiner, claims 1, 3 and 7 do not recite, for example, a LDD region. While Yudasaka '260 may, as the Examiner notes, "provide teaching for these features," it is not proper to turn to the disclosure of Yudusaka '260 for purposes of making a double-patenting rejection. Accordingly, the rejection should be withdrawn.

Applicant submits that all claims are in condition for allowance.

Enclosed is a $180 check for late submission of an information disclosure statement fee. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

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